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**CENTRAL FAX CENTER****JUL 09 2007****Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A track-and-hold circuit having an input signal ( $V_{in}$ ) and an output signal ( $V_s$ ), a bootstrap switch (14a) having as its inputs a clock signal and an input signal ( ~~$v_{in}$~~  $V_{in}$ ), said input signal ( $v_{in}$ ) of said bootstrap switch (14a) being connected to said output signal ( $V_s$ ) of said circuit via level shifting (20) and buffering means (30), characterized in that said input signal ( $v_{in}$ ) of said bootstrap switch (14a) comprises said output signal ( $V_s$ ) of said circuit; said track-and-hold circuit further comprising a capacitor (12), said input signal ( $V_{in}$ ) being connected to said capacitor (12) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit, said bootstrap switch (14a) having as an output to said switch (10), a clock signal ( $clk_{boot}$ ) equal to  $V_{in} + V_{dd}$ .
2. (currently amended) A track-and-hold circuit according to claim 1, including two or more bootstrap switches (14a, 14b), the input signal ( $v_{in}$ ) of each of which is connected to said output signal ( $V_s$ ) of said circuit via said level shifting (20) and buffering means (30).
3. (original) A track-and-hold circuit according to claim 1, wherein said buffering means (30) comprises a MOS transistor.
4. (original) A track-and-hold circuit according to claim 3, wherein said MOS transistor (30) is a PMOS transistor.
5. (canceled)

6. (original) A track-and-hold circuit according to claim 5, further comprising one or more dummy switches (16) which are clocked in anti-phase to said switch (10) connecting said input signal (Vin) to said capacitor (12).

7. (original) A track-and-hold circuit according to claim 6, wherein said input signal (Vin) is connected to said dummy switches (16) via a bootstrap switch (14b), having as an additional input an anti-phase clock signal.

8. (original) An analog-to-digital converter including a track-and-hold circuit according to claim 1.

9. (original) An integrated circuit including an analog-to-digital converter according to claim 8.